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| FORM PTO-1449 (REV. 7-80) | U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE | ATTY. DOCKET NO. NIT-304 | SERIAL NO. |
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U.S. PATENT DOCUMENTS

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| | AA | | | | | |
| | AB | | | | | |
| | AC | | | | | |
| | AD | | | | | |
| | AE | | | | | |
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FOREIGN PATENT DOCUMENTS

| | DOCUMENT | DATE | COUNTRY | CLASS | SUBCLASS | TRANSLATION YES | NO |
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| | AL | | | | | <input type="checkbox"/> | <input type="checkbox"/> |
| | AM | | | | | <input type="checkbox"/> | <input type="checkbox"/> |
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| | AO | | | | | <input type="checkbox"/> | <input type="checkbox"/> |
| | AP | | | | | <input type="checkbox"/> | <input type="checkbox"/> |

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

| | | |
|----|----|---|
| TT | AR | Kume et al, "Flash Memory Technology", Oyou Butsuri, Vol. 65, p. 1114, 1996. |
| TT | AS | J.D.Bude et al, "EEPROM/Flash Sub 3.0V Drain-Source Bias Hot Carrier Writing", IEEE International Electron Device Meeting 1995, p. 989-991. |
| TT | AT | Ogura et al, "Low Voltage, Low Current, High Speed Program Step Split Gate Cell with Ballistic Direct Injection for EEPROM/Flash", IEEE International Electron Device Meeting, 1998, pp. 987-990. |

EXAMINER *T. A. Frese* DATE CONSIDERED *08/02*

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| AO | | | | | | <input type="checkbox"/> <input checked="" type="checkbox"/> |
| AP | | | | | | <input type="checkbox"/> <input checked="" type="checkbox"/> |

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, etc.)

| | | |
|----|----|---|
| TT | AR | T. Jung et al, "A 3.3V 128Mb Multi-Level NAND Flash Memory for Mass Storage Application", IEEE International Solid-State Circuit Conference 1996, pp. 32-33, 1996. |
| | | |
| TT | AS | M. Lorenzini et al, "A Dual Gate Flash EEPROM Cell with Two-Bit Storage Capacity", IEEE Transactions on Components, Packaging, and Manufacturing Technology Part A, Vol. 20, No. 2, p. 182, 1997. |
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| TT | AT | |
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EXAMINER

Talgar

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